

FORM PTO-1449 (MODIFIED)

LIST OF PUBLICATIONS FOR
APPLICANT'S INFORMATION
DISCLOSURE STATEMENT

Applicant(s): H.S. Nagesh et al.
 Case: 10-26-12-10-40
 Serial No.: 10/785,352
 Filing Date: February 24, 2004
 Group: 2661

U.S. PATENT DOCUMENTS

EXAMINER				FILING DATE
INITIAL	DOCUMENT NO.	DATE	NAME	IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

EXAMINER				TRANSLATION	
INITIAL	DOCUMENT NO.	DATE	COUNTRY	CLASS/SUBCLASS	YES NO

OTHER DOCUMENTS

EXAMINER		
INITIAL	REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.

- /A.G./ 1. I. Keslassy et al., "Maintaining Packet Order in Two-Stage Switches," Proceedings of IEEE Infocom, 10 pages, New York, 2002.
- /A.G./ 2. E. Blanton et al., "On Making TCP More Robust to Packet Reordering," pp. 1-11, July 24, 2001.
- /A.G./ 3. S. Iyer et al., "Making Parallel Packet Switches Practical," Proceedings of IEEE Infocom, 8 pages, 2001.
- /A.G./ 4. C-S. Chang et al., "Load Balanced Birkhoff-Von Neumann Switches, Part II: Multi-Stage Buffering," pp. 1-23, August 29, 2001.

Examiner /Ankit Gandhi/

Date Considered

07/23/2007

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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- /A.G./ 1. S. Keshav et al., "Issues and Trends in Router Design," IEEE Communication Magazine, 15 pages, 1998.
- /A.G./ 2. C-S. Chang et al., "Load Balanced Birkhoff-von Neumann Switches, Part I: One-stage Buffering," Computer Communications, pp. 1-25, 2001.
- /A.G./ 3. L.G. Valiant, "A Scheme for Fast Parallel Communication," SIAM Journal of Computing, Volume 11, No. 2, pp. 350-361, 1982.
- /A.G./ 4. ITU-T Recommendation G.7042/Y.1305 - Corrigendum 1, "Link Capacity Adjustment Scheme (LCAS) for Virtual Concatenated Signals," 16 pages, 2002.
- /A.G./ 5. ITU-T Recommendation G.7042/Y.1305, "Link Capacity Adjustment Scheme (LCAS) for Virtual Concatenated Signals," 24 pages, 2001.
- /A.G./ 6. ITU-T Recommendation G.707/Y.1322, "Network Node Interface for the Synchronous Digital Hierarchy," 184 pages, 2000.

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